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10/657,141	09/09/2003	Masao Murade	116802	1897

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EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/657,141	MURADE, MASAO	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-19* is/are pending in the application.

4a) Of the above claim(s) *14-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,11-13 and 19* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/19/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claims 14-18 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on January 14, 2005.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the driving circuit that drives the scanning lines, the data lines, and the pixel electrodes must be shown or the feature(s) canceled from the claim(s) (claim 4). Note that the drawings show a separate scanning line driving circuit and a data line driving circuit. They do not show a single driving circuit that drives both the scanning lines and the data lines. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the

renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 4, the limitation "a driving circuit arranged on either the counter substrate or the substrate that drives the scanning lines, the data lines, and the pixel electrodes" renders the claim indefinite. Claim 1 already defines a data line driving circuit. Therefore, it is unclear if this limitation refers to an additional data line driving circuit. Furthermore, it is unclear how a single driving circuit can drive the scanning lines, the data lines, and the pixel electrodes. The instant application discloses both a scanning line driving circuit and a data line driving circuit. For the purposes of this Office Action, it is considered that the data line and scanning line driving circuits together form the claimed driving circuit, even though they are not connected.

Regarding claim 11, the limitation "a data line driving circuit" renders the claim indefinite. Claim 1 already defines a data line driving circuit. Therefore, it is unclear if this limitation refers to an additional data line driving circuit.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-7, 9, 13, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Sasaki (US Pat. 6,100,865).

Regarding claims 1 and 6, Figure 3 of Sasaki discloses an electro-optical device, comprising: data lines (D1-D4) extending in a predetermined direction; scanning lines (G1-G4) crossing the data lines; a display region including pixel electrodes (P11-P44) and pixel switching elements (T11-T44) disposed in correspondence with intersections of the scanning lines and the data lines, image signals from the data lines being supplied to the pixel electrodes through corresponding pixel switching elements; capacitor electrode wiring lines (lines connected between capacitors C1-C4 and GND, shown at top of figure) extending in a direction crossing the data lines; a data line driving circuit 107/108 (col. 4, lines 55-57) that drives the data lines, the data line driving circuit being located at one side of the display region; and capacitors (C1-C4) located at the opposite side of the pixel area than the data line driving circuit, the capacitors including first electrodes including conductive layers connected to the data lines without any

switching element between the conductive layers and the data lines, the capacitors including second electrodes that include other conductive layers connected to the capacitor electrode wiring lines (through resistances R1-R4). The limitation "the capacitors reducing or preventing an unstable change in image signal supplied to the pixel electrodes by the data lines" is merely a recitation of intended use that does not structurally/patentably distinguish the claimed invention over the prior art. Regarding claim 6, Figure 3 of Sasaki also discloses the capacitors are provided separately from any inherent capacitance of any transistor.

Regarding claim 3, the limitation "the capacitor electrode wiring lines having a fixed potential" is merely a functional/intended use limitation that does not structurally distinguish the claimed invention over the prior art. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). The capacitor electrode wiring lines are capable of having a fixed potential if the appropriate voltage is applied.

Regarding claim 4, Figure 3 of Sasaki discloses an LCD device (col. 4, line 51). An LCD device must have a substrate and a counter substrate facing the substrate. Sasaki discloses a counter electrode (opposed electrode) capacitively coupled to the pixel electrodes (P11-P44) through the liquid crystal layer (col. 3, lines 40-41). Therefore, the counter electrode must be on the counter substrate, facing the pixel electrodes. Figure 3 of Sasaki discloses a driving circuit (107/108 and 101) arranged on either the counter substrate or the substrate (circuit must be

arranged on one of the substrates) that drives the scanning lines, the data lines, and the pixel electrodes. It is inherent that a power source (first power source) supplies a potential to the counter electrode and that another power source (second power source) supplies a potential to the driving circuit 107/108. Therefore, the capacitor electrode wiring lines are indirectly connected to the second power source through resistors R1-R4, capacitors C1-C4, and data lines D1-D4. The limitations "that supplies a fixed potential to..." and "to have a fixed potential" are merely functional/intended use limitations that do not structurally distinguish the claimed invention over the prior art.

Regarding claim 5, the capacitor electrode wiring lines shown in Figure 3 of Sasaki must be made of a low resistance material in order to conduct a current.

Regarding claim 7, Figure 3 of Sasaki discloses the data line driving circuit 107/108 (col. 4, lines 55-57) being located at one end of the data lines (D1-D4); and a test circuit 109 that checks the operation of the electro-optical device at the other end of the data lines (col. 4, line 66 – col. 5, line 3).

Regarding claim 9, the product-by-process limitation "such that during manufacturing, the capacitor electrode wiring lines and the data lines can be formed in the same step" does not structurally distinguish the claimed invention over the prior art.

Regarding claim 13, it can be considered that the data lines (D1-D4) shown in Figure 3 of Sasaki are divided into a plurality of groups. For instance, D1 and D2 are one group, and D3 and D4 are another group. The limitation "to which image signals are simultaneously supplied" is merely a recitation of intended use that does not structurally the claimed invention over the prior art.

Regarding claim 19, the electro-optical device discloses in Figure 3 of Sasaki must be part of an electronic apparatus.

Claims 1, 3-6, 8, 9, 13, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishii.

Regarding claims 1 and 6, Figures 1-4(D) of Ishii disclose an electro-optical device, comprising: data lines 30 extending in a predetermined direction; scanning lines 20 crossing the data lines; pixel electrodes 55 and pixel switching elements 50 disposed in correspondence with intersections of the scanning lines and data lines, image signals from the data lines being supplied to the pixel electrodes through corresponding pixel switching elements; capacitor electrode wiring lines 29 extending in a direction crossing the data lines; and capacitors (intersections between data lines 30 and capacitor wiring lines 29) including, as first electrodes, conductive layers (part of data line) connected to the data lines without any switching element between the conductive layers and the data lines, the capacitors including second electrodes (part of capacitor lines 29) that include other conductive layers connected to the capacitor electrode wiring lines. Note that a capacitance inherently exists between the data lines 30 and the capacitor electrode wiring lines 29 at the intersection between these lines, since there must be some type of dielectric layer between the overlapping wiring lines 29 and 30 (otherwise they would short each other out). Therefore, it can be considered that the intersections are capacitors, wherein the portions of the lines where the overlap occurs are the respective capacitor electrodes. Figure 1 of Ishii also discloses a data line driving circuit 60 that drives the data lines 30 at one end of the

data lines, the capacitors (at least some) being provided at the other end of the data lines. Regarding claim 6, the capacitors are provided separately from any inherent capacitance of any transistor. Note the above inherent capacitance is between adjacent wiring layers and is not part of a transistor.

Regarding claim 3, the limitation "the capacitor electrode wiring lines having a fixed potential" is merely a functional/intended use limitation that does not structurally distinguish the claimed invention over the prior art. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). The capacitor electrode wiring lines 29 of Ishii are capable of having a fixed potential if the appropriate voltage is applied.

Regarding claim 4, Figures 1-4(D) of Ishii disclose a substrate 10; a counter substrate (col. 7, lines 59-61) facing the substrate; a counter electrode formed on the counter substrate (col. 7, lines 59-61) and arranged to face the pixel electrodes; and a driving circuit 60/70 arranged on the substrate 10 that drives the scanning lines, the data lines, and the pixel electrodes. It is inherent that a power source (first power source) supplies a potential to the counter electrode and that another power source (second power source) supplies a potential to the driving circuit 70. Ishii discloses the capacitor electrode wiring lines 29 are connected to scanning line driving circuit 70, and therefore are connected to the same power source as the driving circuit (second power source). The limitations "that supplies a fixed potential to..." and "to have a fixed

potential" are merely functional/intended use limitations that do not structurally distinguish the claimed invention over the prior art.

Regarding claim 5, it is inherent that the capacitor electrode wiring lines 29 are made of a low resistance material in order to perform their intended function.

Regarding claim 8, Figures 1-4(D) of Ishii disclose storage capacitors (not labeled) connected to the pixel electrodes and the pixel switching elements. The product-by-process limitation "such that, during manufacturing, at least some of the members forming the capacitors can be formed..." does not structurally/patentably distinguish the claimed invention over the prior art.

Regarding claim 9, the product-by-process limitation "such that, during manufacturing, the capacitor electrode wiring lines and the data lines can be formed in same step", does not structurally/patentably distinguish the claimed invention over the prior art.

Regarding claim 13, it can be considered that the data lines 30 shown in Figure 1 of Ishii are divided into a plurality of groups. The limitation "to which image signals are simultaneously supplied" is merely a recitation of intended use that does not structurally the claimed invention over the prior art.

Regarding claim 19, it is inherent that the electro-optical device disclose by Figures 1-4(D) of Ishii is part of an electronic apparatus.

Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Tada et al. (JP 09-265110, hereinafter Tada).

Regarding claim 12, Figures 5-7 of Tada disclose an electro-optical device comprising: data lines 42 extending in a predetermined direction; scanning lines 41 crossing the data lines; pixel electrodes 40 and pixel switching elements 43 disposed in correspondence with intersections of the scanning lines and the data lines; and capacitors 54 including first electrodes 77 (also labeled as 52 in Figure 6) including conductive layers connected to the data lines without any switching elements between the conductive layers and the data lines, portions of the first electrodes of the capacitors being wider than the data lines (shown in Figure 6).

Allowable Subject Matter

Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 11 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed October 19, 2005 and December 1, 2005 have been fully considered but they are not persuasive.

Applicant argues that Ishii "fails to disclose all of the features recited in independent claims 1 and 6 because the mere crossing of data lines 30 with capacitor lines 29 in a wiring schematic does not translate to the actual crossing of those wires in a real-world circuit, or in the creation of an inherent capacitance". However, Figure 4(A) of Ishii shows those same elements in a diagram that is not simply a wiring schematic. Figure 4(A) of Ishii discloses the data lines 30 crossing the wiring lines 29 (not labeled in this figure, but clearly shown as the uppermost horizontal line). This figure is a representation of the real-world circuit and device layout, therefore it can be relied upon for showing the overlap of the two lines. As stated previously, when two conductive lines overlap as shown in Figure 4(A), there will be a capacitance between those lines as long as there is a dielectric layer in between. There must be some type of dielectric between lines 30 and 29, otherwise those lines would be shorted together and the device would not function as intended. Applicant further argues that, "it cannot be assumed that data lines 30 and capacitor lines 29 are sufficiently close to result in an inherent capacitance". The examiner respectfully disagrees. The substrates in an LCD device such are the one disclosed by Ishii are very thin. Therefore, the distance between lines 30 and lines 29 can be assumed to be minimal. Regardless of the distance between these lines, there will always be at least some degree of capacitance. The examiner has established a basis in fact and/or technical reasoning to reasonably support the determination of inherency. The burden is now on Applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of the claimed product (see MPEP 2112(IV) and 2112(V)). Furthermore, the inherent capacitance (regardless of how small it may be) is capable of reducing, at least to some degree, an unstable change in image signal supplied to the pixel electrodes by the data line.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew C. Landau

February 6, 2006